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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,369	09/22/2003	Hee-Sok Pang	053785-5151	4918

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MORGAN LEWIS & BOCKIUS LLP
1111 PENNSYLVANIA AVENUE NW
WASHINGTON, DC 20004

EXAMINER

RIELLEY, ELIZABETH A

ART UNIT PAPER NUMBER

2879

DATE MAILED: 04/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/665,369

Applicant(s)

PANG ET AL.

Examiner

Elizabeth A. Rielley

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 March 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Response to Amendment

Amendment filed 3/22/06 has been entered and considered by the Examiner. Currently, claims 1-19 are pending in the instant application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-3 and 6-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hosokawa (US 20020011783) in view of Eida et al (US 6344712) and Himeshima et al (US 20030011305).

In regard to claims 1, 10, 14, 16, and 18, Hosokawa ('783) teaches a transmissive-type organic electroluminescent display device (61-67) comprising forming a substrate (10) including sub-pixel regions thereon (31; paragraph 14), forming an array element in each sub-pixel area that includes thin film transistors (14); forming a partition wall at a border portion between adjacent sub-pixel regions made of an insulating material (25; figure 3; paragraph 160); forming a first electrode (22) made of a transparent conductive material in each sub-pixel region between adjacent partition walls (paragraph 21);

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wherein the first electrode (22) contact the adjacent partition wall (25; see figure 3) forming an organic electroluminescent layer on the first electrode in each sub-pixel region between the adjacent partition walls (24); forming a second electrode (20) made of a transparent conductive material on the organic electroluminescent layer (paragraph 14); and encapsulating the substrate including the second electrode by forming a passivation layer covering the second electrode (58; figure 8; paragraphs 93 and 94).

Hosokawa ('783) does not teach that the transparent conductive material of the first electrode is disposed on an upper surface of the partition wall and that the partition wall is made of a transparent, organic material.

Eida ('712) teaches the transparent conductive material of the first electrode 33; figure 19a; column 9 lines 23-27; column 29 lines 45-48) is disposed on an upper surface of the partition wall (22; see figure 19a) in order to improve viewing quality (column 2 lines 51-56). Hence it would have been obvious at the time of the invention to one of ordinary skill in the art to combine the OLED of Hosokawa ('783) with the electrode configuration of Eida ('712). Motivation to combine would be to improve viewing quality.

Both Eida ('712) and Hosokawa ('783) are silent regarding the limitation of the partition wall made from a transparent, organic material. Himeshima et al (US 20030011305) discloses a partition wall for an organic electroluminescent device made from a transparent (paragraphs 58 and 115), organic (paragraph 76) material in order to increase the brightness of the OLED. Hence, it would have been obvious at the time of the invention to one of ordinary skill in the art to combine to OLED of Hosokawa and the electrode configuration of Eida ('712) with the transparent material for the partition wall as taught by Himeshima et al ('305). Motivation to combine would be to increase the brightness of the OLED.

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In regard to claim 2, Hosokawa ('783) teaches the organic electroluminescent layer is made of a high molecular material (paragraphs 116-117).

In regard to claim 3, Hosokawa ('783) teaches the partition wall forms an opening having a rectangular shape corresponding to the sub-pixel region (figure 4b; paragraphs 151-152).

In regard to claim 6, Hosokawa ('783) teaches the partition wall is formed only in a first direction at a border portion between adjacent sub-pixels (figure 3).

In regard to claim 7, Hosokawa ('783) teaches a method of forming a fluorescent layer by roll coating (paragraph 244).

In regard to claim 8, Hosokawa ('783) teaches the organic electroluminescent layer is formed by an ink jet method (paragraph 287).

In regard to claim 11, Hosokawa ('783) teaches the first electrode is an anode electrode (paragraph 190) and the second electrode is a cathode electrode (paragraph 166), where in the second electrode includes a metallic thin film having a low work function contacting the organic electroluminescent layer (paragraphs 166 and 168).

In regard to claim 12, Hosokawa ('783) teaches the metallic thin film includes aluminum (paragraph 168).

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In regard to claim 13, Hosokawa ('783) teaches an electrode made of indium zinc oxide (paragraph 138).

In regard to claim 15, Hosokawa ('783) teaches both electrodes made of indium zinc oxide (paragraphs 38, 138 and 191).

In regard to claim 17, Hosokawa ('783) teaches the organic electroluminescent layer is formed by an ink jet method (paragraph 287).

In regard to claim 19, Hosokawa ('783) teaches both electrodes made of indium zinc oxide (paragraphs 38, 138 and 191).

Claims 4, 5, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hosokawa ('783) in view of Eida et al (US 6344712) and Himeshima et al (US 20030011305) as applied to claim 1 above, and further in view of Morii et al (US 20020109456).

In regard to claim 4, Hosokawa/Eida/Himeshima disclose all the limitations set forth, as described above, except that the partition wall forms an opening having a circular shape corresponding to the sub-pixel region so that the ink lies well in the sub-pixel sections (paragraph 47). Morii ('456) teaches the partition wall forming an opening having a circular shape corresponding to the sub-pixel region (paragraph 47; figure 1). It would have been obvious at the time of the invention to combine to OLED of Hosokawa/Eida/Himeshima with the circular shape Morii et al ('456) so that the ink lies well in the sub-pixel sections.

In regard to claim 5, Hosokawa ('783) teaches the organic electroluminescent layer is formed by an ink jet method (paragraph 287).

In regard to claim 9, Hosokawa/Eida/Himeshima disclose all the limitations set forth, as described above, except the partition wall has a thickness within a range of 1 μm to 8 μm . Morii et al ('456) teaches the thickness of an organic partition wall is 2 μm in order to produce a more efficient lighting device. Hence it would have been obvious at the time of the invention to one of ordinary skill in the art to combine the OLED of Hosokawa/Eida/Himeshima with the partition wall thickness of Morii. Motivation to combine would be to produce a more efficient lighting device.

Response to Arguments

Applicant's arguments filed 3/22/06 have been fully considered but they are not persuasive.

In regard to Applicant's argument that the prior art of record fails to teach the electrode contacts the adjacent partition walls, the Examiner respectfully disagrees. Hosokawa teaches a first electrode (22) contact the adjacent partition wall (25) in figure 3. Hence, the prior art of record discloses all the limitation sets forth in the current claims.

The Applicant asserts that there is no motivation for combining the transparent partition wall of Himeshima et al ('305) with the electrode configuration of Eida ('712). However, the Examiner is combining the electrode configuration of Eida ('712) with the OLED of Hosokawa ('783) in order to improve the viewing quality of the display (column 2 lines 51-56) as well as combining the transparent

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partition wall for an OLED as taught by Himeshima et al ('305) with the OLED of Hosokawa ('783) in order to increase the brightness of the OLED. This is *not* combining the transparent partition wall of Himeshima with the entire OLED of Eida, rather, it is a combination of the transparent wall of Himeshima with the OLED device of Hosokawa and the electrode configuration of Eida. Also, in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Himeshima et al (US 6469439) also teach transparent partition walls for an OLED.

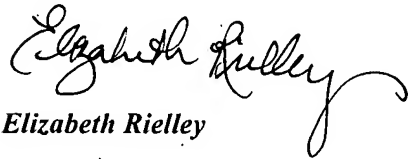
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elizabeth A. Rielley whose telephone number is 571-272-2117. The examiner can normally be reached on Monday - Friday 7:30 - 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimeshkumar Patel can be reached on 571-272-2457. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained

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from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Elizabeth Rielley

Examiner
Art Unit 2879

ms 4/3/06
MARICELI SANTIAGO
PRIMARY EXAMINER